ABSTRACT OF THE DISCLOSURE

In a power management semiconductor device or analog semiconductor device having a CMOS and a resistor, a conductivity type of a gate electrode of the CMOS is P-type as to both an NMOS and a PMOS, a short channel and a low threshold voltage are possible since an E-type PMOS is surface channel type, the short channel and the low threshold voltage are possible since a buried channel type NMOS is extremely shallow for the reason that arsenic having a small diffusion coefficient can be used as an impurity for threshold control, and the resistor used in a voltage dividing circuit or CR circuit is formed of polycrystalline silicon thinner than the polycrystalline silicon of the same layer as the gate electrode or a thin film metal. Thus, the power management semiconductor device or analog semiconductor device, which is advantageous in terms of cost, manufacturing period and element performance in comparison with the conventional CMOS with an N+polycrystalline silicon gate single polarity or the same polarity gate CMOS in which a channel and a gate electrode have the same polarity, can be realized.